PROVISIONAL

ADC MOD. 7420/G

USERS' GUIDE

REV.2

I N D E X

WARNING

It is strongly recommended that the NIM module be not inserted with the Power Supply "ON" in order to prevent the reliability of the electrolytic and Tantalum condensers used from being degraded.

HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER MOD. 7420

Section 1

INTRODUCTION

1.1. General Description

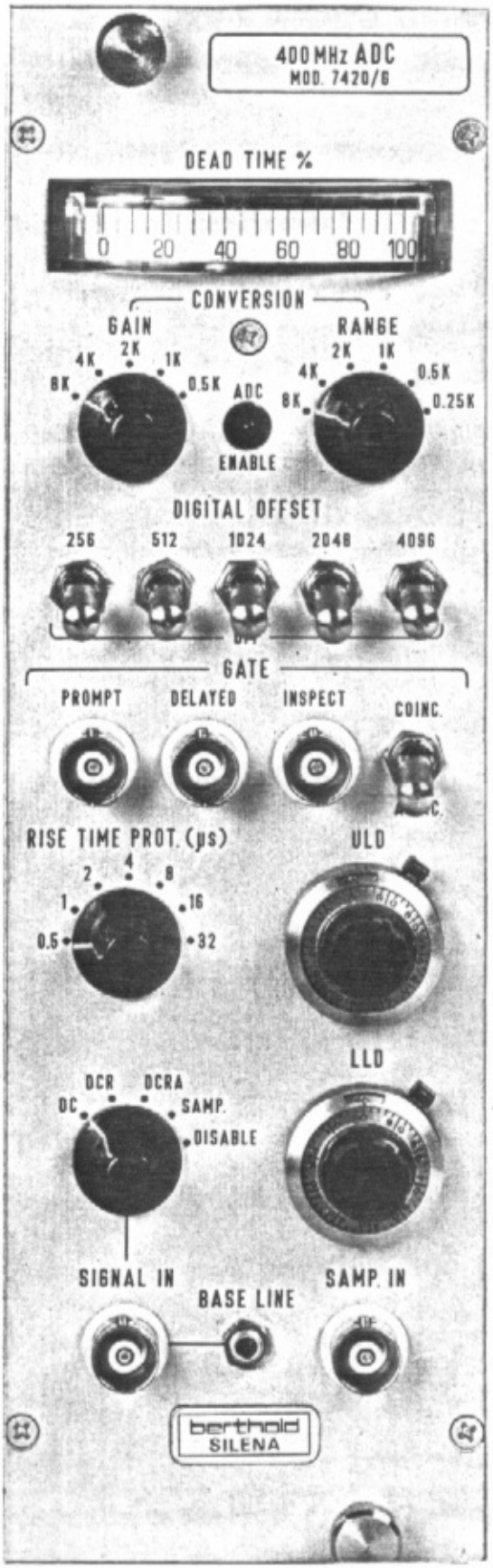
The Model 7420 is a high-speed, Wilkinson type analog-to-digital converter providing a data acquistion efficiency enhanced by a 400 MHz digitizing rate.

The Model 7420 is a double-width NIM standard module.

1.2. Applications

Its unique combination of high conversion speed (average 0.9 µsec on 1024 channels and 6.9 µsec. on 8192 channels), optimum differential and integral linearity and excellent stability make the Model 7420 the ideal ADC for applications in nuclear and X-ray spectroscopy.

It is also used for periodic sampling of DC or slowly varying DC signals (SVA) in all those applications where linearity, stability and conversion speed are prime requisites.


400 MHz ADC
MOD. 7420/B
DEAD TIME %
0 20 40 60 80 100
CONVERSION
GAIN
8K 4K 2K 1K 0.5K
ADC
ENABLE
RANGE
8K 4K 2K 1K 0.5K 0.25K
DIGITAL OFFSET
256 512 1024 2048 4096
GATE
PROMPT
DELAYED
INSPECT
COINC.
RISE TIME PROT. (µs)
0.5 1 2 4 8 16 32
ULD
LLD
DC DCR DCRA SAMP. DISABLE
SIGNAL IN
BASE LINE
SAMP. IN
berthold
SILENA

Section 2

SPECIFICATIONS

2.1. INPUT

2.1.1. Input Signal Requirements :

- Polarity	: positive or bipolar (positive portion leading)
- Range	: 20 mV to 8,2 Volt into 1000 Ohm
- Rise Time	: 50 ns to 32 µs (longer on request)
- Fall Time	: 50 ns. to 200 µs
- Width	: 0,5 µs minimum

2.1.2. Input Mode (switch-selectable)

- DC coupling
- AC with passive dc restorer
- AC with active dc restorer
- Sampling

2.1.3. Conversion Start Mode (switch-selectable)

- Rise Time Protection (RTP) switch-selectable from 0,5 to 32 µs.
- Peak Detector

2.1.4. Coincidence/Anticoincidence

Pulse or DC level requirements

- False	: $0\ V < V_F < 0,5\ V$
- True	: $2\ V < V_T < 5\ V$
Input	: front-panel BNC connector
Coincidence Inspect	: front-panel BNC connector, at which there is available the RTP pulse, (see par. 4.3.10)

2.2. PERFORMANCE

2.2.1. ADC

- Conversion time

- Variable	: (0.64 + 0.0025 N) µS where N is the address generated for a given amplitude (N includes digital backbias, if any)
- Fixed	: 21 µs with 8 K of conversion gain 11 µs with 4 K of conversion gain 5.8 µs with 2 K of conversion gain 3.2 µs with 1 K of conversion gain 1.9 µs with 0,5 K of conversion gain
- ADC Dead Time	: R.T.P. or Time-to-Peak + Conversion Time + Memory Storage Time
- Internal Data Buffer (Derandomizer)	: allows the ADC to convert a newly acquired input while simultaneously transferring the last data conversion to the memory storage unit.
- Integral non linearity	: $\leq$ 0.025% over 99.5% of range measured with 2 µs flat top pulse $\leq$ 0.035% over 99.5% of range measured with 0.5 µs flat top pulse
- Differential non linearity	: $\leq \pm$ 0.3% over 99.5% of range
- Gain Stability	$\leq \pm$ 0.002% /°C
- Baseline stability	: $\leq$ 100 µV/°C
- Clock rate	: 400 MHz crystal-controlled
- Count Rate Shift (in DC input mode)	: less than 1/2 channel at rates up to 50 KHz

2.2.2. SVA Mode (Sampled Voltage Analysis)

- Sampling Time	: preset by RTP switch from 0.5 to 32 µs
- Sampling Pulse Requirements (Front-panel BNC connector)	
- False	: $0V < V_F < 0.5$ V
- True	$2V < V_T < 5$ V
- Width	: $\geq$ 100 ns.

2.2.3. SCA

Timing	: Output pulse generated when input pulse falls through the LLD setting. Open collector TTL output with 1K pull up resistor to +5V. The pulse width is 0.2 µs.

2.3. CONTROLS

Conversion Gain	: Five-position rotary switch selects full scale selection of input signal. Selections of 8192, 4096, 2048, 1024 or 512 channels of 8,2 V.
Conversion Range (Digital Overflow)	: Six-position rotary switch selects 8192, 4096, 2048, 1024, 512 or 256 addresses for storage.
Digital backbias	: Five two-position switches provide digital backbias from 0 to 7936 channels in 256 channel steps.
Dead Time	: Two-position switch selects variable dead time or fixed dead time.
Coincidence	: Two-position switch provides Coincidence/ Anticoincidence selection. Two independent BNC inputs are available for selection of prompt or delayed coincidence.
Dead Time Meter	: Indication of average percentage of time ADC is busy.
Lower Level Discriminator	: Ten-turn locking potentiometer sets lower limit of ADC and SCA window; continuously adjustable from 20 mV to 8,2 V.
Opper Level Discriminator	: Ten-turn potentiometer sets upper limit of ADC and SCA window; continuously adjustable from 8,2 V to 20 mV.

Rise Time Protection	: Seven-position rotary switch selects Rise Time Protection from 0,5 µs to 32 µs
Baseline	: Twenty-turn potentiometer sets the zero level of ADC from 0 to 200 mV
Input Mode	: Five-position rotary switch selects the input mode of ADC (see 2.1.2.). The last position disables the ADC.

2.4. OUTPUTS (see also par. 3.3. and par. 6)

Data (J_3 and $J_{3'}$)	: 37-pin connector containing gated binary $2^0 - 2^{12}$ buffered data and control signals to memory unit.
SCA	: Rear-panel BNC connector for SCA output pulse (see 2.2.3.)
Stabilizer	: 9-pin connector containing control analog signal from stabilizer to ADC.
Total Dead Time	: Provides positive TTL logic level during ADC dead time (Rear-panel BNC connector).
Conversion time	: Output signal. It is low during ADC's conversion time.
Inspect	: At this front-panel BNC connector there is available the Rise Time Protection Pulse for controlling coincidence/anticoincidence timing.

2.5. CONNECTOR TYPES

2.5.1. FRONT PANEL

Signal in	: BNC (isolated)
Sampling in	: BNC (isolated)
Prompt Coincidence	: BNC (isolated)
Delayed Coincidence	: BNC (isolated)
Coincidence Inspect (RTP signal)	: BNC (isolated)

2.5.2. REAR PANEL

Data	: 37-contact male connector Type CANNON DCSPB - 37 P
Total Dead Time	: BNC (isolated)
SCA Output	: BNC (isolated)
Conversion Binary	: BNC (isolated)
Spectrum Stabilizer (J_6)	: 9 contacts female connector type CANNON DE - 9S

2.6. POWER REQUIREMENTS

+ 24 V	: 0.16 A
- 24 V	: 0.13 A
+ 6 V	: 0.2 A
- 6 V	: 1.1 A

2.7. DIMENSIONS : Single two-width NIM standard module.

2.8. WEIGHT : 2 kg.

Section 3

CONTROLS, INDICATORS, ADJUSTMENT AND CONNECTORS

3.1. General

Complete understanding of the purpose of the various controls and connectors is required for the proper operation of the ADC and it is recommended that this Section be read before proceeding with the operation of the instrument.

3.2. Front Panel (refer to Fig. 3.2.)

3.3. Rear Panel (refer to Fig. 3.3. and par. 6 for Connector Signal List)

3.4. Internal

3.4.1. Printed Card 889 (refer to Fig. 3.4.1.)

This card can be accessed by removing the left side panel of the ADC.

- Derandomizer (Internal Data Buffer) : Two-position switch. When set to "ON" activates the Data Buffer. This buffer allows the ADC to convert newly acquired input while simultaneously transferring the last data conversion to the memory storage unit.

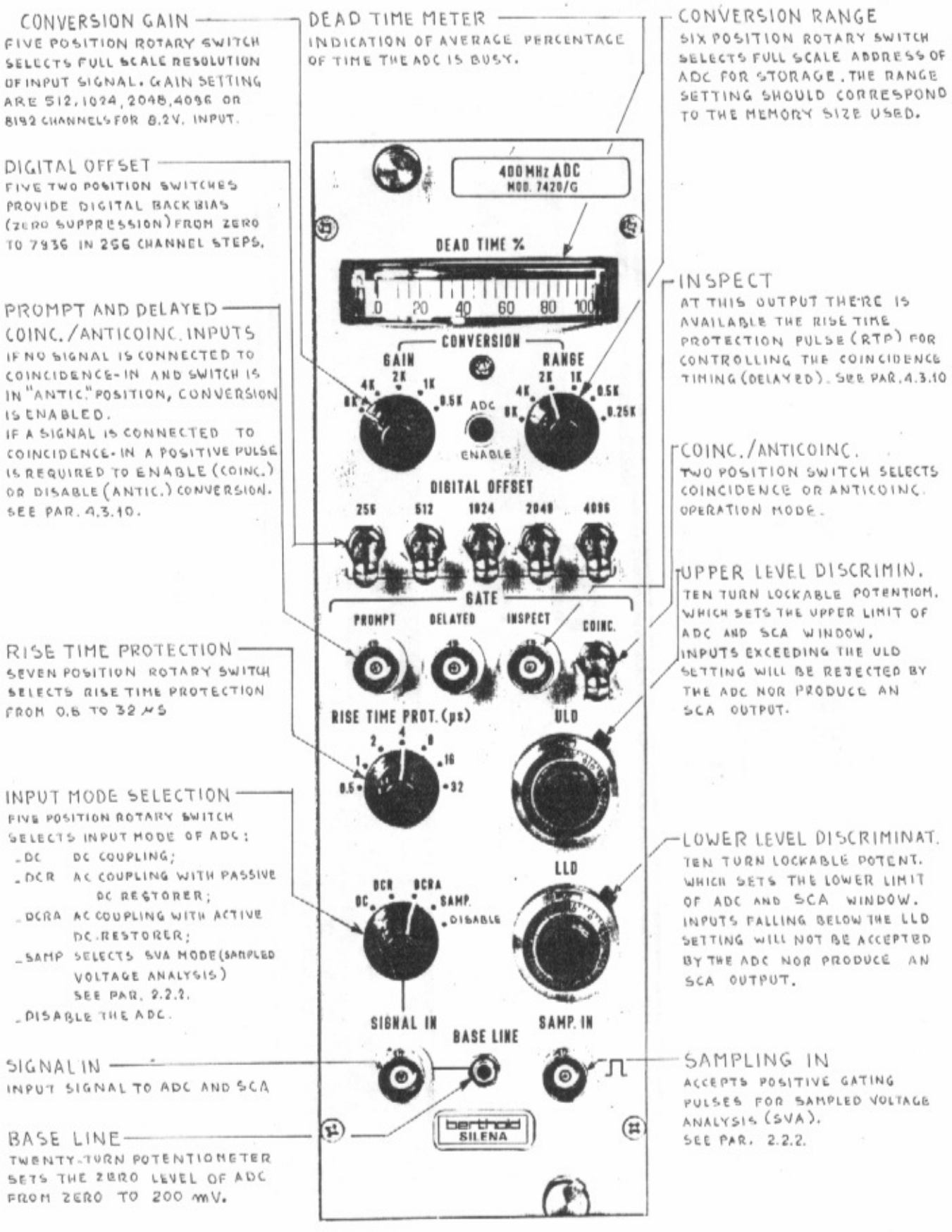


FIG. 3.2 FRONT PANEL

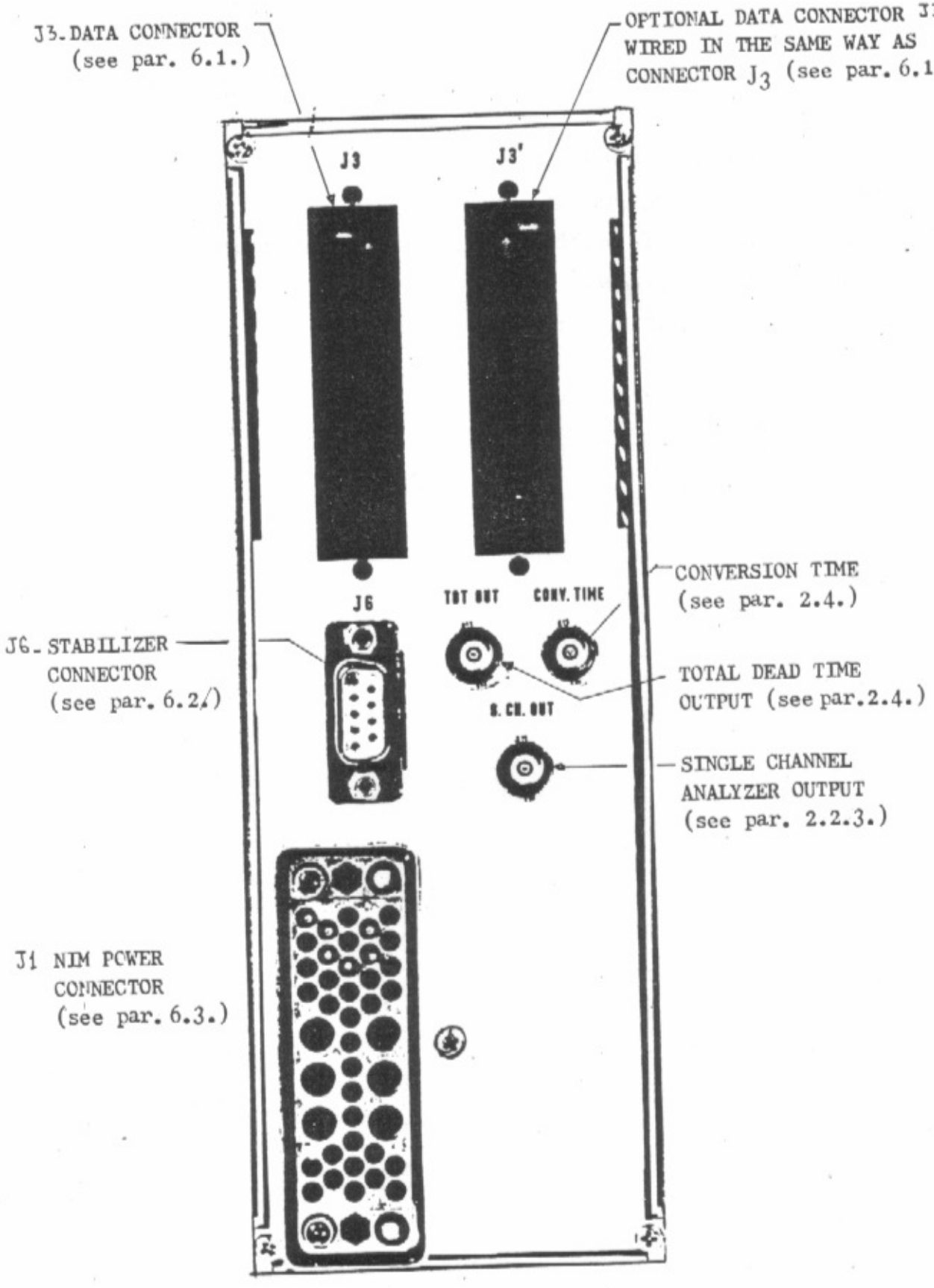


Fig. 3.3. - REAR PANEL

3.4.2. Front Panel Printed Card (refer to Fig. 3.4.2.)

Dead Time Selection : Two-position slide switch selects fixed or variable dead time.

Conversion Start Mode: Two-position slide switch selects the conversion start mode of ADC. (see par. 4.3.2.).

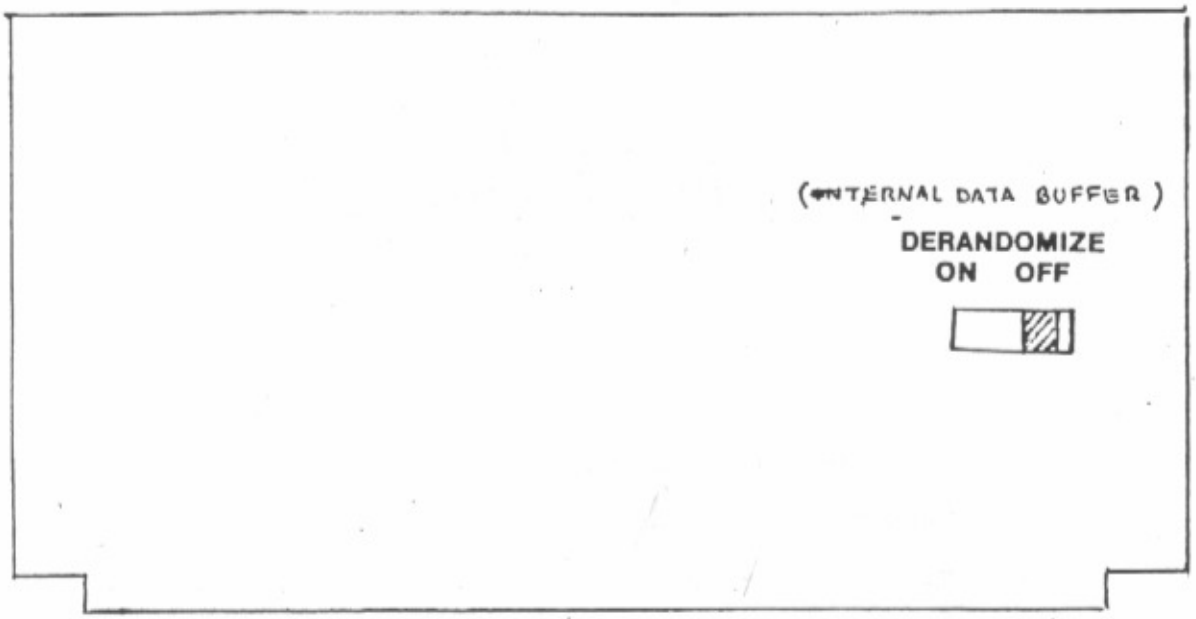


FIG. 3.4.1 _ PRINTED CARD # 889 _ INTERNAL CONTROL

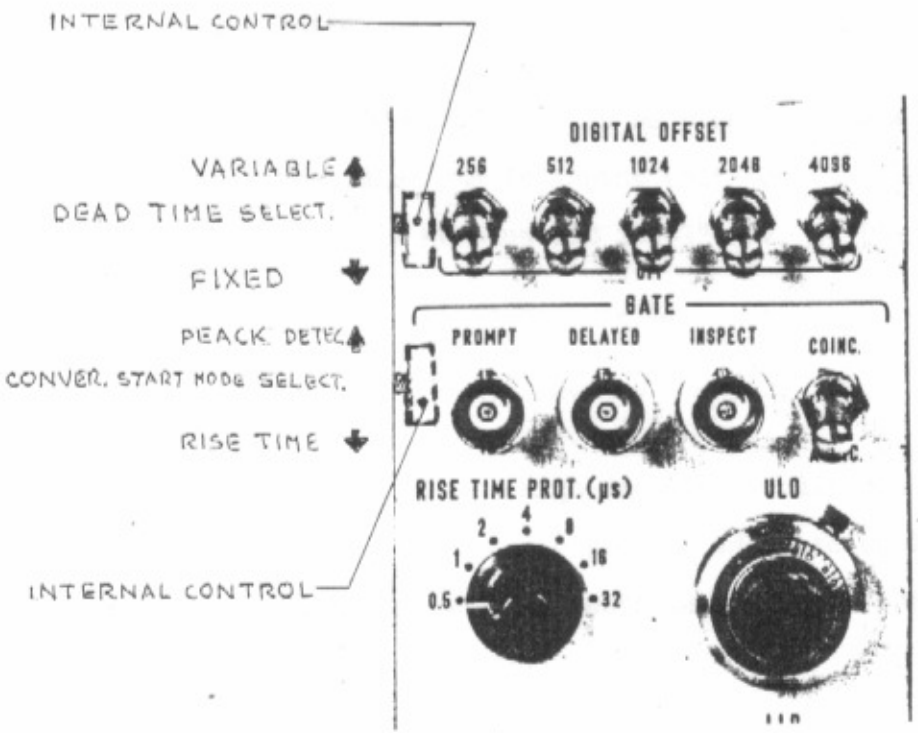


FIG. 3.4.2 _ FRONT PANEL PRINTED CARD. INTERNAL CONTROLS.

Section 4

OPERATING INSTRUCTIONS

4.1. General

This Section provides details on the operation of the ADC. Since it is difficult to determine the exact system configuration in which the unit will be used, explicit operating instructions cannot be given. However it is recommended that this Section and Section be read before proceeding with the operation of the instrument.

4.2. Installation

The ADC Mod. 7420 can be plugged into a NIM Bin Power Supply providing the following voltages (as per "Standard Nuclear Instrument Modelus TID 20893" Rev. 2, Jan. 1968) :

+ 24 - 24 +6 - 6

For power requirements, see par. 2.6.

Because of the high-density circuit package, ample air flow must be assured to provide adequate cooling as specified in "Standard Nuclear Instrument Modules" page 7 - point 5.

4.3. PULSE HEICHT ANALYSIS

4.3.1. Prior to initiating a spectrum measurement some preliminary calibration checks and set-ups are required.
Generally these preliminary set-ups are carried out with the analyzer operating in "DATA-IN" and the mesure in progress being viewed on the CRT.

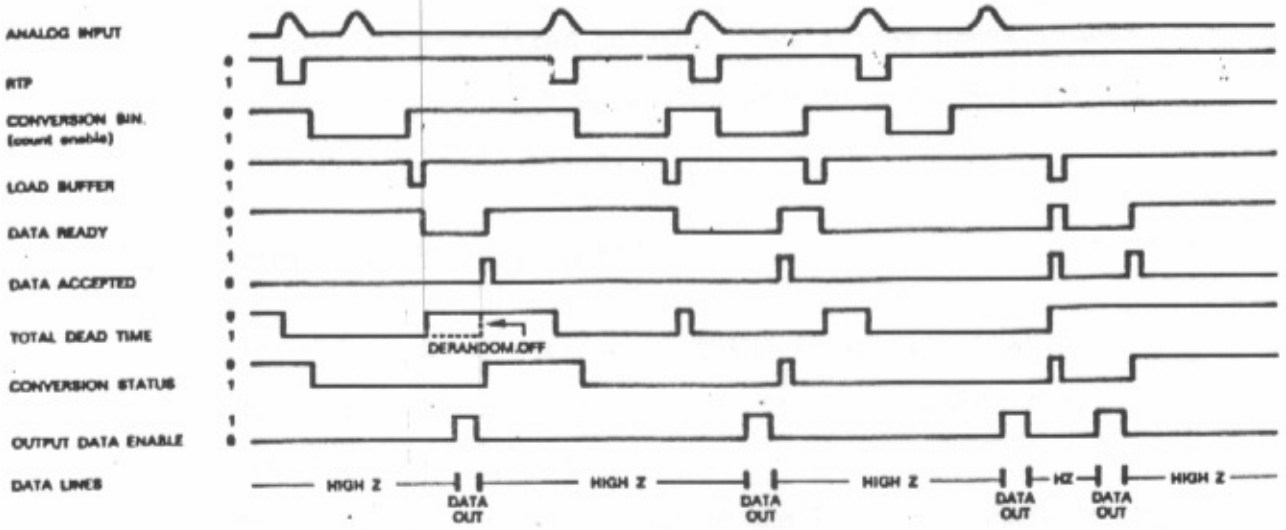
After the preliminary set-up and check procedure has been completed, stop the analyzer pressing the STOP pushbutton and clear the memory.
Pressing again the "DATA IN" pushbutton causes the true analysis run to initiate.

4.3.2. Rise Time Protection (RTP) Adjustment

To measure the maximum amplitude of a pulse the ADC can operate in two different modes selectable by internal switch.

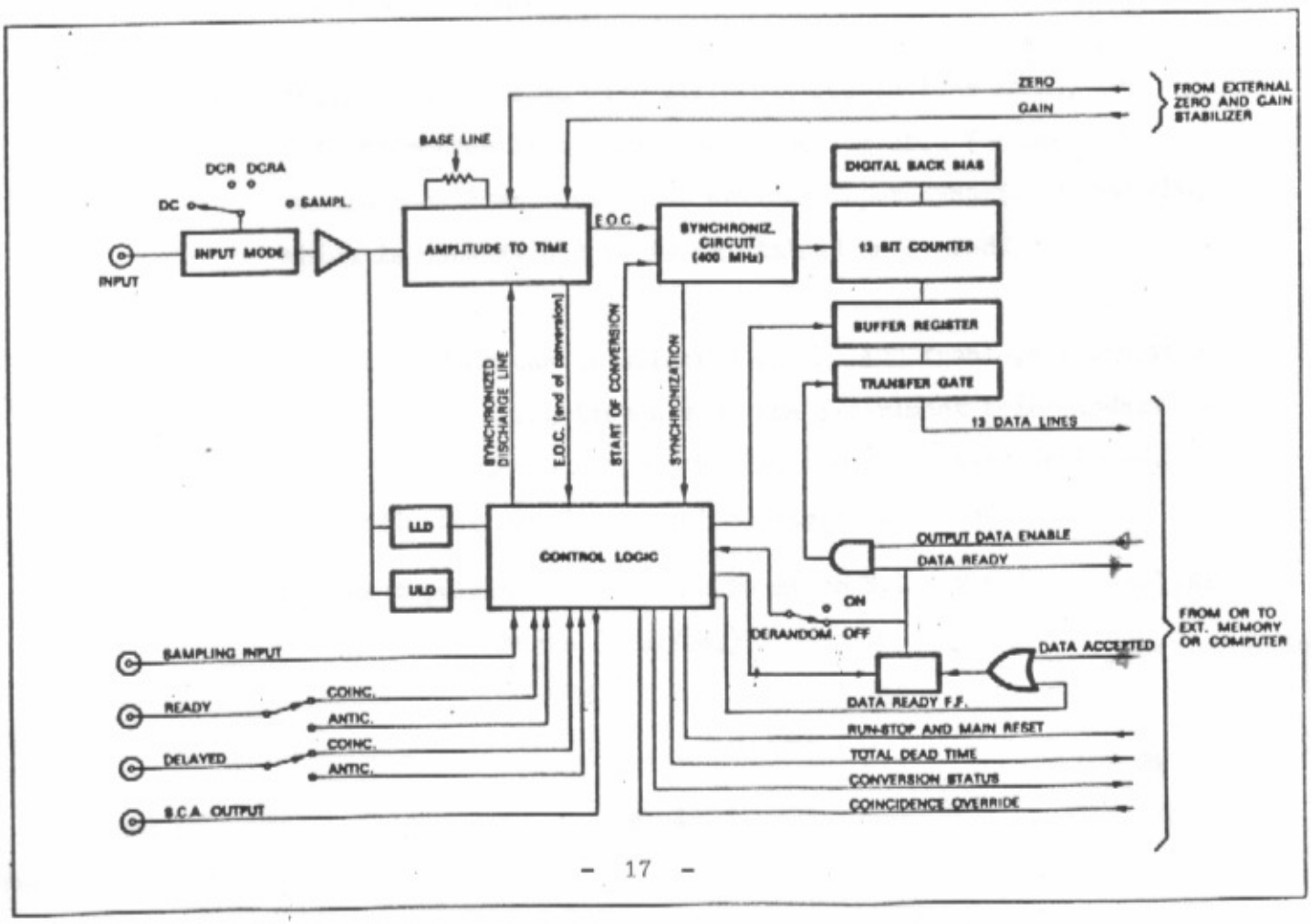
Peak Detector Mode

In this mode of operation, the analog-to-digital conversion of the input pulse initiates at the instant when the pulse, after it has reached its top amplitude, starts decreasing. This instant is detected by a peak detector circuit fitted at the ADC's input.
This mode of operation allows spectra analysis to be performed independently of the rise time of the pulses being analysed.
In fact, the pulse rise time may vary as a function of the time constants selected in the amplifier.
Time constants selection depends to some extent on the shape of the pulses from the preamplifier.



ADC MOD. 7420 - TIMING DIAGRAM

A.D.C. MOD. 7420 - GENERAL BLOCK DIAGRAM



Use of the Peak Detector is not recommended in the presence of long tailed pulses, since it may cause serious time jitters occurring at the beginning of the dead time and loss of resolution.

4.3.2. Rise Time Protection Mode

In this mode of operation, pulse conversion initiates after a ΔT delay with respect to the starting instant of the pulse rise time.
This instant is determined by the lower threshold switching (see Lower Level Discriminator Adjustment).
This delay, which is designated as "Rise Time Protection" must be selected by the operator on the front-panel of the ADC (see par. 3.2.) in such a way that it may last longer than the pulse rise time.

4.3.3. ADC's Conversion Gain Selection

The ADC may operate with different resolutions in mV/channel independently of the memory portion used for spectra accumulation, even though the maximum input dynamic of the ADC, which is usually 8,2 V, is maintained unaltered.

The resolution can be selected on the ADC front-panl according to the special requirements of the experiment being undertaken and the actual dynamic of the input pulses being analysed.
The following resolution values may be selected:

8 K Input pulses in the range 20 mV to 8,2 V will be analysed on 8192 channels (1 mV/ch.)

4K Input pulses in the range 20 mV to 8,2 V will be analysed on 4096 channels (2 mV/ch)

2K Input pulses in the range 20 mV to 8, 2 V will be analysed on 2048 channels (4 mV/ch.)

1K Input pulses in the range 20 mV to 8, 2 V will be analysed on 1024 channels (8 mV/ch.)

0,5 Input pulses in the range 20 mV to 8,2 V will be analysed on 512 channels (16 mV/ch).

4.3.4. ADC's Conversion Range Selection

After the resolution in mV/ch. for ADC operation has been selected (see par.4.3.3), it is necessary to adjust the digital output from the ADC so that it can be compatible with the memory portion of the analyzer being used for spectra accumulation.

To do this, adjust the "Conversion Range" rotary switch fitted on the ADC front-panel.

8K	corresponding to	13 output bits	equal to 8192 channels
4K	corresponding to	12 output bits	equal to 4096 channels
2K	corresponding to	11 output bits	equal to 2048 channels
1K	corresponding to	10 output bits	equal to 1024 channels.
0,5K	corresponding to	9 output bits	equal to 512 channels.
0,25 K	corresponding to	8 output bits	equal to 256 channels.

4.3.5. Digital Back-Bias Selection

Whenever it is required to analyse a spectrum with a preset energy range and a resoltuion in mV/ch not compatible with the memory range of the MCA, it is possible to introduce a digital back-bias so as to make the spectrum accumulated in the memory and shown on the CRT correspond to the energy range of interest. In this way, spectrum analysis is performed in two successive times and with different back-bias values.

The introduction of the digital back-bias allows the energy axis to be displaced to the left by a ΔE value given by the following relation :

$$\Delta E = N \cdot \text{resolution}$$

Where N is the backbias value in channels and the resolution is expressed, for example in KeV/ch.

4.3.6. Lower Level Discriminator (LLD) Adjustment

To minimize the conversion dead time, the lower level discriminator should be set in such a way that all pulses having an amplitude less than that of the pulses classified in the first channel are rejected.

To do this, set first the analyzer to "DATA IN" with all input pulses fed to the ADC. Then rotate the LLD potentiometer completely counterclockwise (LLD disabled).
After this, rotate again the LLD potentiometer clockwise until the content of the first few channels being viewed on the CRT is not longer incremented.
For a more accurate visual inspection, the full scale should be set to 10^2 or 4×10^2.
At this point, to obtain a correct adjustment of the LLD the potentiometer should be turned in the opposite direction by about a quarter of turn.

4.3.7. Upper Level Discriminator (ULD) Adjustment

To minimize the conversion dead time, the upper level discriminator should be set in such a way that all pulses exceeding the last channel are rejected.

To do this, set first the analyzer to "DATA IN". Then rotate the ULD potentiometer completely clockwise (ULD disabled).
After this, rotate again the potentiometer counterclockwise until the content of the last few channels being viewed on the CRT is not longer incremented.

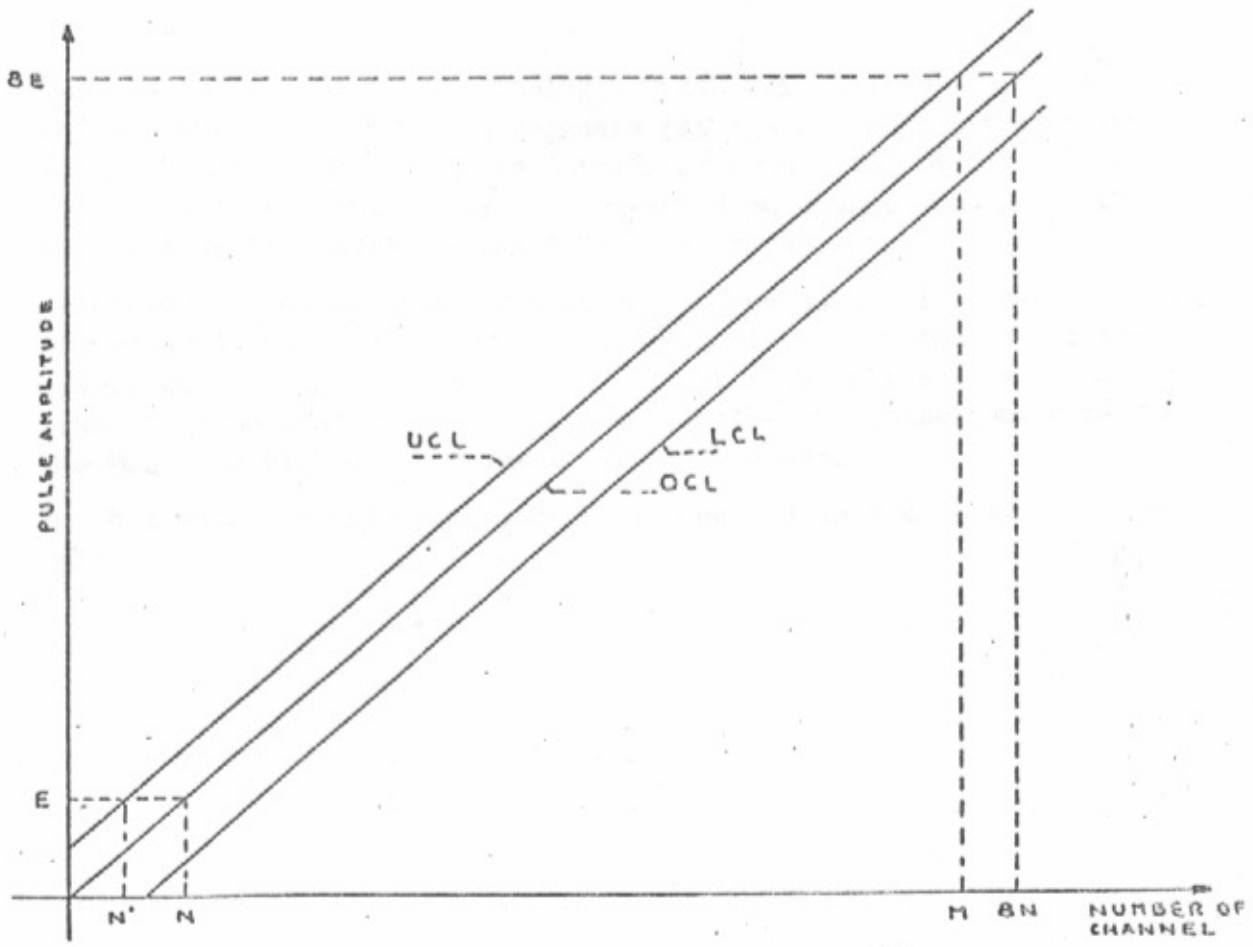
For a more accurate inspection, the full scale should be set to 10^2 or 4×10^2.
At this point, to obtain a correct adjustment of the ULD, the potentiometer should be turned in the opposite direction by about a quarter of turn.

4.3.8. ADC's Baseline Adjustment

In some cases, it is convenient to calibrate the ADC so that data conversion may occur on the line crossing the origin (OCL Line) (see Diagram). It should be noted that in this case the pulse amplitude, and consequently the energy is directly proportional to the channel number. That is to say, if the E energy peak is classified into channel N, the 8E energy peak will be classified into channel 8N.

This direct proportionality considerably simplifies all calculations required to determine the energies of unknown peaks.

To cause data conversion to occur on the OCL conversion line, check that the backbias is switched off (all switches disactivated).



Assuming that due to incorrect setting of the "BASELINE" potentiometer BL. data conversion takes place on line U.C.L., a pulse having a width E will be classified into channel N and a pulse having a width 8E into channel M.

If M is greater than 8N, potentiometer BL should be turned clockwise (counterclockwise) so that pulses are routed to a higher channel. Then, the memory is cleared again and energy pulses E and 8E are measured. If the two pulses are not classified into two channels, the second of which is 8 times higher than the first, potentiometer BL must be adjusted until this condition is met.
Zero crossing of the conversion line is therefore obtained by successive approximations.
After this calibration has been performed, no change will occur even if the backbias is introduced, provided that the number of biased channels is added to the number of the channel in which the pulse has been stored.

That is to say, if a pulse having a width E is stored in channel 100 and a backbias equal to 785 channels (at the ADC output the channel number is 785 + 100 = 885) is introduced by setting the digital backbias, a pulse having a width 2E will be converted on channel 885 x 2 = 1770 and will be stored into channel 1770 - 785 = 985.

Referring to the diagram given above, let us assume that the pulse to be converted has a 20 mV amplitude, which is the minimum value linearly convertible. If "RANGE" is set to 2048, the conversion constant will be 2 mV/channel, and consequently the pulse converted on the OCL line will be stored into the 10th channel.

In this case, no information will be recorded in the first 9 channels.

4.3.9. Energy Calibration

To perform energy calibration with a known value (for example 1 KeV/channel) a spectrum with at least a low and a high energy peak must first be entered into the analyzer memory. After the spectrum has been entered, the current energy calibration should be calculated. This will most probably be different from the desired energy calibration.

Using the calibration value obtained, calculate the channel into which the first spectrum has to be entered. At this point adjust the baseline potentiometer so as to cause the peak to be moved to the desired channel.
This will cause the energy/channel straight line to cross the origin.

Then adjust the amplifier gain such that the high energy peak will move to the desired channel.
Check that the low energy peak is in the correct position. If this is not the case, repeat the above procedure using the new calibration value.

Example

Let us consider a spectrum with the Am 24 peak at 60 KeV and a spectrum with the CS 137 peak at 662 KeV. We wish to calibrate the analyzer at 1 KeV/channel. Let us assume that the barycentre of the first peak is located at channel 57 instead of channel 60 and the second at channel 818 instead of channel 662. The difference between the channels is given by 818-57 = 743. The difference in energy is given by 662-60 = 602 KeV. Therefore, the current calibration in KeV/channel will be 602 KeV/743 channels = 0,81 KeV/channel.

The channel corresponding to a 60 KeV/energy will be given by 60/0,81 = 74.

At this point, rotate the Baseline (BL) potentiometer clockwise until the peak is moved to channel 74.

In this way the energy scale zero will be calibrated.

Then, adjust the gain of the Linear Amplifier until the second peak will be moved to channel 662. At this point, check that the lower level peak is located at channel 60. If so, repeat the above procedure using the new calibration values obtained.

4.3.10. Coincidence and Anticoincidence (Prompt or Delayed)

It is possible to condition analysis of input pulses to the ADC by applying logic signals externally generated.

The ADC has two basic operation modes:

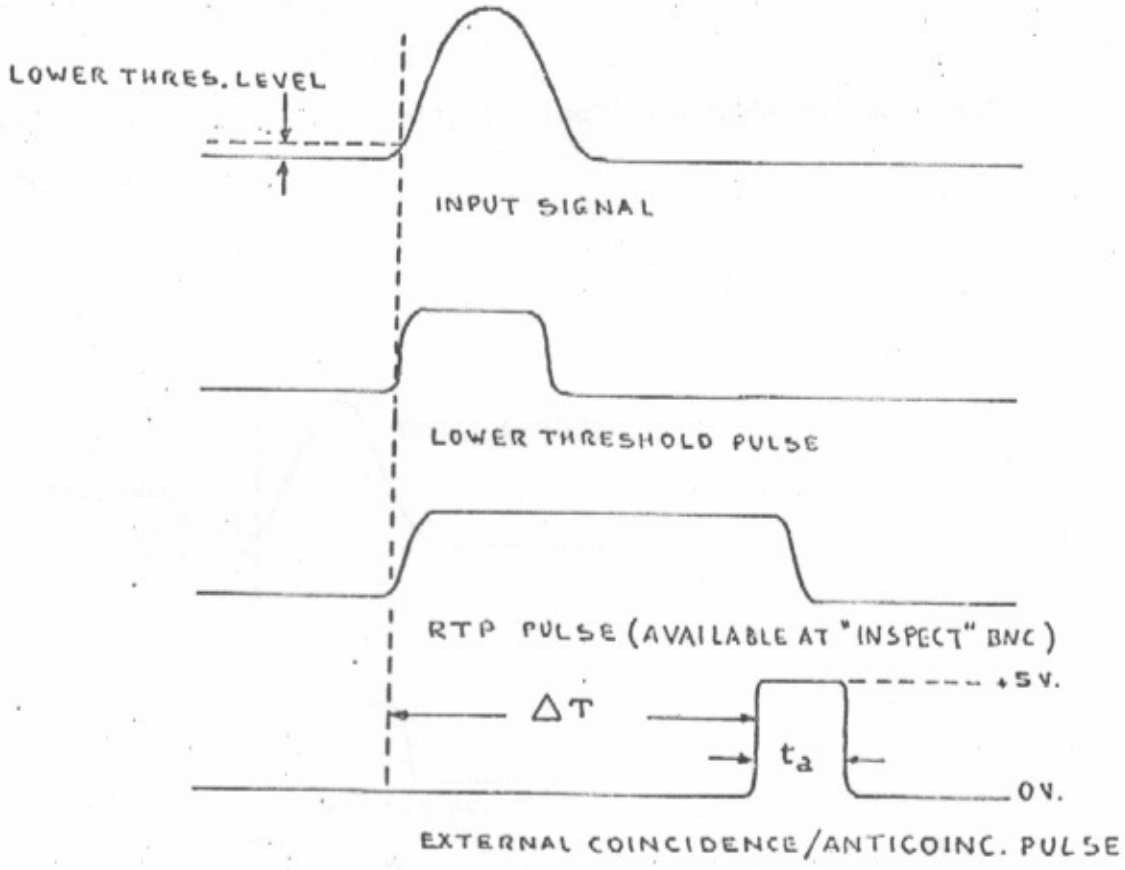
- Coincidence (prompt or delayed)
- Anticoincidence (prompt or delayed)

Selection between the coincidence and anticoincidence mode is performed by setting the appropriate front-panel switch.

Two input BNC connectors for prompt and delayed coincidence signals are available on the ADC front-panel. An output BNC connector is also provided. Available at this connector is the pulse signal generated internally (Rise Time Protection - RTP). The delayed coincidence or anticoincidence pulse must coincide with the leading adge of the RTP.

Delayed Coincidence/ Anticoincidence

The pulse or dc level requirements are the same as for the Prompt Coincidence/Anticoincidence.



EXTERNAL COINCIDENCE/ANTICOINC. PULSE

The ΔT delay elapsing between the leading edge of the input pulse and the leading edge of an externally applied pulse should be shorther than the preset "Rise Time Protection" by 50 ns approximately. That is to say:

$$\Delta T \leq RTP - 0.05 \ \mu sec.$$

where RTP indicates the value of the "Rise Time Protection" in microseconds. The length t_a of the externally applied pulse should be preset such that it will cover completely the leading edge of the RTP.

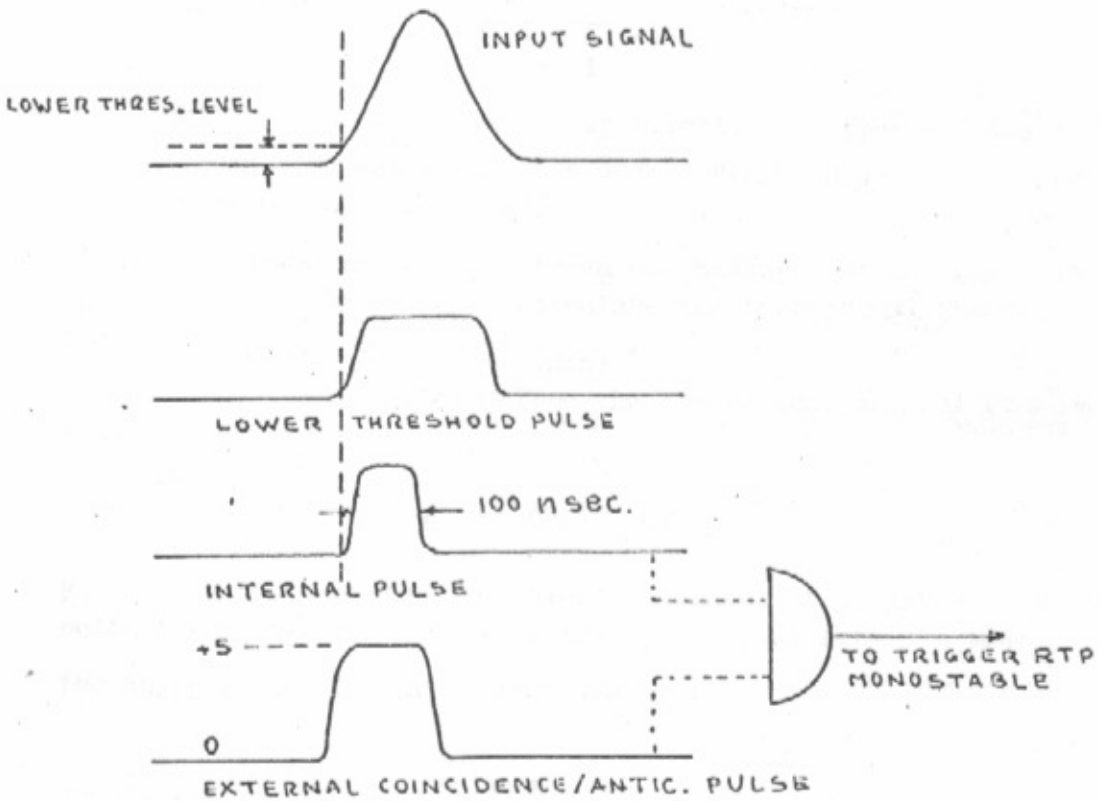
In anticoincidence mode the prompt coincidence input (if not used) must be grounded.

Prompt Coincidence/Anticoincidence

Pulse or dc requirements for coincidence or anticoincidence are as follows:

Reference Level	: 0	Without external connection of BNC the level is +5 V. with an input impedance of 3.3 KOhm.
Polarity	: positive	
Amplitude	: 5 V	
Width	: see drawing	

In anticoincidence mode the delayed coincidence input (if not used) must be grounded.



5 _ MEASUREMENT OF INTEGRAL LINEARITY

Perform a series of measurements sending in pulses (or voltages if operating in sampling mode) progressively increasing in amplitude at regular time intervals (for example every 0,5 V) with an accuracy of 0,1 mV approx.

Then write down the numbers of the channels in which each pulse has been converted in the column "MEASURED CHANNEL" of a Table. If pulse conversion occurs in two adjacent channels, compute the barycentre according to the following formula :

$$CM = C_{Low} + \frac{Counts_{C_{High}}}{Counts_{C_{Low}} + Counts_{C_{High}}}$$

Calculate the average increment (INC) in channels between one measurement and the next one according to the following formula :

$$INC = \frac{CM_{(max)} - CM_{(min)}}{n - 1}$$

where $CM_{(max)}$ and $CM_{(min)}$ are respectively the upper and lower channel in which the measurement has been carried out, and n is the number of measurements performed.

Once the average increment between one measurement and the next one is known, it is possible to calculate the theoretical channel CT assuming $CT_{(min)}$ equal to $CM_{(min)}$.

At this point the deviation from the theoretical channel can be calculated from :

$$\Delta C = CM - CT$$

Plotting a graph of the ΔC values obtained, it is possible to calculate the deviation C_{max} from the theoretical straight line.

The integral non linearity is given by :

$$INL\ (°/_{oo}) = \pm \frac{1}{2} \cdot \frac{\Delta C_{max}}{CM_{(max)} - CM_{(min)}} \cdot 1000$$

EXAMPLE OF MEASUREMENT OF THE INTEGRAL LINEARITY OF THE ADC MOD. 7420 USING A PULSE GENERATOR TYPE P.B.4. MANUFACTURED BY BERKELEY NUCLEONIC CORP.

Pulse Characteristics

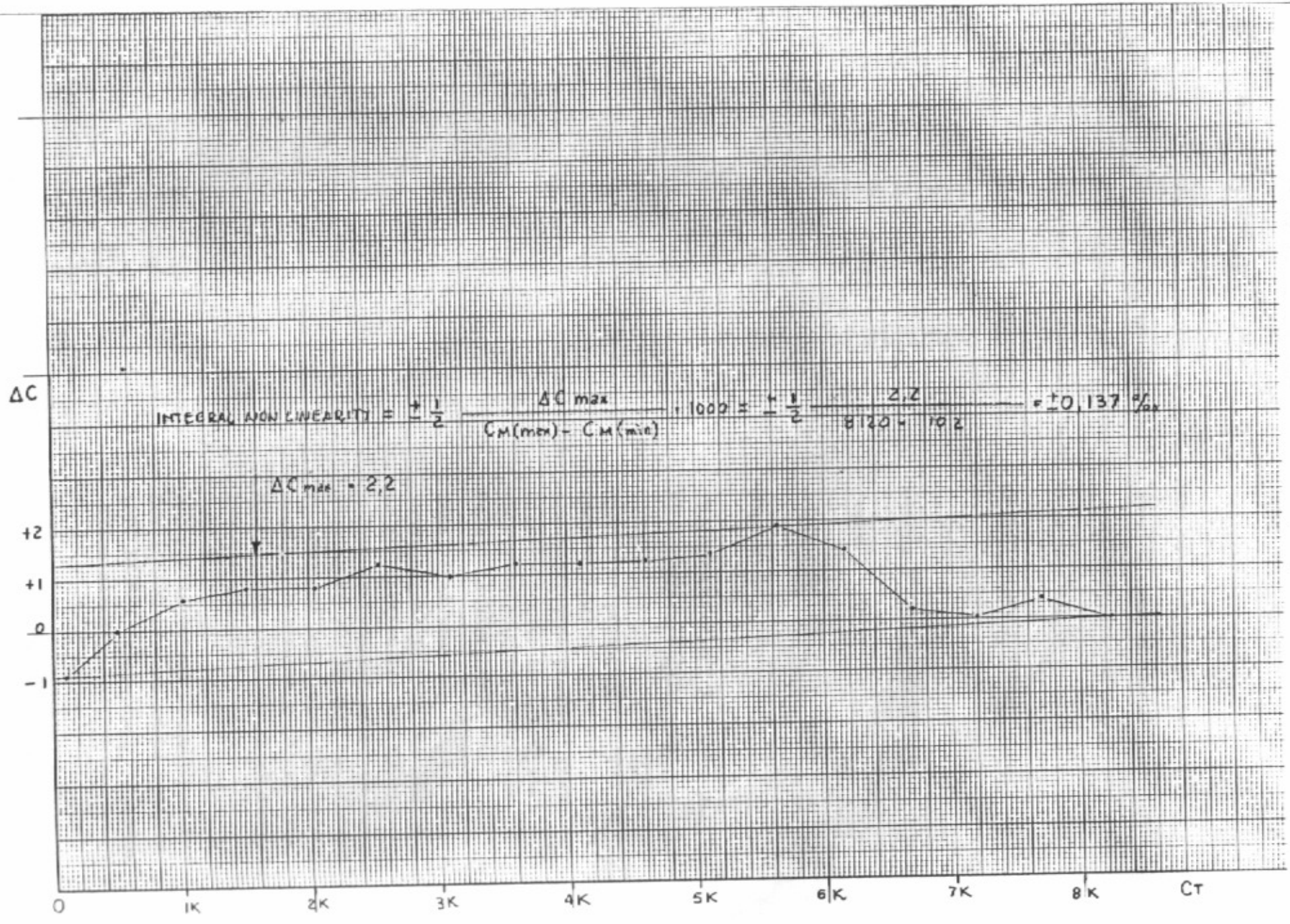
Polarity : Positive
Top Width : 2 μsec
Rise Time : 0,5 μsec

Vin	Cm	Ct	ΔC
8	Cm (max) 8120	Ct(max) 8120	0
7,5	7613	7612,6	+0,4
7	7105,57	7105,2	+0,05
6,5	6598	6597,8	+0,2
6	6091,8	6090,4	+1,4
5,5	5584,92	5583	+1,92
5	5076,95	5075,6	+1,35
4,5	4569,45	4568,2	+1,25
4	4062	4060,8	+1,2
3,5	3554,62	3553,4	+1,22
3	3047	3046	+1
2,5	2539,82	2538,6	+1,22
2	2032	2031,2	+0,8
1,5	1524,61	1523,8	+0,8
1	1017	1016,4	+0,6
0,5	Cm (min) 509	Ct(min) 509	0
* 0,1	102,87	103,8	-0,93

$$INC = \frac{Cm\ (max) - Cm\ (min)}{n-1} = \frac{8120 - 509}{15} = 507,4$$

* In this measure $\Delta Vin = 0,4$ V

$\Delta CT = 0,8$ INC


ΔC
INTEGRAL NON LINEARITY = ± 1/2 ΔC max / (CM(max) − CM(min)) · 100 = ± 1/2 2,2 / 8120 − 102 = ± 0,137 %
ΔC max = 2,2
+2
+1
0
−1
0
1K
2K
3K
4K
5K
6K
7K
8K
CT

6. CONNECTOR SIGNAL LIST

6.1. J_3 and J_3' - Data

The J_3' connector is of the same type as the J_3 one and is provided, on request, for special uses of the ADC; All outputs, except data, are open collector with 3.3. KOhm pull-up resistor to +5 V.

Pin	Mnemonic	Signal Description
1	$\overline{2^0}$	
2	$\overline{2^1}$	
3	$\overline{2^2}$	Gated, Binary Address Data
4	$\overline{2^3}$	
5	$\overline{2^4}$	Logic 1 = 0V
6	$\overline{2^5}$	
7	$\overline{2^6}$	Logic 0 = +5V
8	$\overline{2^7}$	
9	$\overline{2^8}$	Fan-out = 5 TTL
10	$\overline{2^9}$	
11	$\overline{2^{10}}$	Three state output 3.3 KOhm pull
12	$\overline{2^{11}}$	up resistor to +5
13	$\overline{2^{12}}$	
14	$\overline{\text{RTP}}$	Rise time protection output (Active Low)
15	$\overline{\text{TOT OUT}}$	ADC total dead time - Output signal to gate live time circuitry or to control storage period (Active Low)
16	$\overline{\text{TOT IN}}$	Total dead time in. Input signal to gate the ADC on or off (Active Low for OFF). Pulses in progress prior to beginning of $\overline{\text{TOT IN}}$ will be allowed to continue and finish the output sequence but further pulses will be ignored. This signal if low sets LOW the $\overline{\text{TOT OUT}}$.
17	ADC ENABLE	ADC enable output signal that is LOW if ADC is enabled to operate (ADC ENABLE front-panel indicator illuminated).
18	NC	
19	NC	

Pin	Mnemonic	Signal Description
20	RUN/STOP	Input signal to enable (Active HIGH) the operation of ADC. It is used with SILENA MCA.
21	$\overline{\text{DATA READY}}$ (Flag)	Output signal to memory unit. Signals that a conversion is complete (Active Low)
22	DATA ACCEPT	Input signal from memory unit that acknowledged data acceptance. This pulse resets the flag (Data Ready) (Active High)
23	ENABLE DATA	Input to gate the 13 bit data onto the output lines. This line is active high. If low, the output lines are on high impedance.
24	$\overline{\text{CONVERSION BINARY}}$	Output signal. It is low during ADC's conversion time.
25	$\overline{\text{CONVERSION STATUS}}$	Output signal. Indicates that a conversion has resulted from a coincidence or an anticoincidence (Active Low)
26	$\overline{\text{COINCIDENCE OVERRIDE}}$	Input signal. If low, enables conversion of an input pulse even in the the absence of prompt or delayed coincidence or anticoincidence signal.
27	$\overline{\text{OVERFLOW+UPPER THRESHOLD}}$	Output pulse signal generated on occurrence of the overflow and upper threshold switching. (Active Low) (0.5 us width).
28 ÷ 34	NC	
35	DELAYED COINCIDENCE	Input signal. Can be used for delayed coincidence (Active High); alternately available at the front-panel BNC.
36	GND	Ground
37	NC	

6.2. STABILIZER

Pin	Mnemonic	Signal Description
1	ZERO CORRECTION	Input analog signal from stabilizer used to correct zero.
2	GND	Ground line twisted with zero correc tion line.
3	$\overline{\text{ZERO ENABLE}}$	Input signal to enable the zero cor rection (Active Low)
4	GAIN CORRECTION	Input analog signal from stabilizer to correct gain.
5	GND	Ground line twisted with Gain Correc tion line
6	$\overline{\text{GAIN ENABLE}}$	Input signal to enable the Gain Cor rection (Active Low)
7	$\overline{\text{TDT}}$	Total Dead Time Output (Active Low)
8	$\overline{\text{RESET}}$	Input pulse line from preamplifier to reset pulse conversion in progress on occurrence of the discharge pulses from detector (Active Low)
9	$\overline{\text{RTP}}$	Rise Time Protection Output (Active Low)

6.3. NIM POWER J_1 CONNECTOR

Pin	Mnemonic	Signal Description
10	+ 6 V	
11	- 6 V	
18	+ 5 V	(see Note)
28	+ 24V	
29	- 24V	
34	GND	

NOTE - This pin can be used to feed the ADC with +5V (0.2 A). In this case, the +6V cannot be fed to pin 10.