Model 7423/UHS 8k Ultra High-Speed Spectroscopy

The Model 7423/UHS is an ultra high-speed, highly reliable, digitally corrected subranging analog to digital converter. The excellent differential linearity characteristics of the ADC are from the incorporation of a special design that minimizes the ADC differential non linearity and from the use of the sliding scale method devised by Prof. Emilio Gatti (Nuclear Instruments and Methods Vol. 24, p241 (1963), patented in Europe and U.S.).

The exclusive design eliminates all undesirable effects (peak broadening, etc.) due to ageing effects in the DAC used for the sliding scale corrected ADC.The Model 7423/UHS makes extensive use of integrated circuits: only a few discrete components and no hybrid microcircuits are employed. The Model 7423/UHS is designed for use with SILENA analysers. However, because of its modular design, it can be easily used with many existing data processing systems.

- 8K ADC
- 3uSec conversion time
- Integral non-linearity 0.02% over the top 99.8% of the range
- Differential non-linearity 0.3% over the top 99.8% of the range
- Pulse amplitude analysis and sampling of analog waverforms
- Range factor selection: 1,2,4,8,16,32,64 (mV/ch)
- Conversion range selection: 256, 512, 1k, 2k, 4k or 8k
- Input: either DC or active DC restorer
- Digital back-bias
- Peak detector, rise time protection or delay after peak
- Dead time indicator: 10% FS or 100% FS 20 LED BAR Display
- Lower level and upper level discriminator
- Input for spectra stabilisation
- Designed for easy interfacing to computers
- Differential line driver eliminates ground loop prblems
- Ready coincidence
- True delayed coincidence facility at end of RTP detection or DT coincidence)
- Overflow stored in channel zero (internally selectable)
- Output data lines fully compatible with all SILENA's ADCs
- Fully compatible with all SILENA NIM modules
- No dead time for spectroscopy amplifier pulses
- 0,5 mS shaping and up Gaussian pulse: 0.5 mS shaping

FRONT PANEL CONTROLS

- Conversion Range (Digital Overflow) Six-position rotary switch to select 7936- 4096-2048-1024-512 or 256 quantisation channels respectively for 7936-4096-2048-1024-512 or 256 mV of full scale input pulses
- Range Factor (mV/ch) Seven-position rotary switch to provide data compression of selected conversion range - Compression range is 1, 2, 4, 8, 16, 32 or 64
- Digital Offset Five switches to provide digital offset in steps of 256 channels
- Gate Ready or delayed coincidence or anticoincidence may be used simultaneously. Coincidence delay is selectable in three modes. At peak detection, Rise Time Protection or DT (RTP) after Peak in steps of 0.5 - 1.5 - 3 - 6 - 8 - 16 or 25 mS. Pulse or DC level requirements:
  False OV<VF<0,5V
  True 2V <VT<5V

- To facilitate use of the ADC in the "multiparameter coincidence" mode, a coincidence override input line is provided. If TRUE, it permits conversion of pulses even in the absence or prompt or delayed coincidence or anticoincidence signals.
- LLD (Lower Level Discriminator) Ten-turn potentiometer sets minimum input amplitude acceptance level, continuously adjustable from 20 mV to 8 V
- ULD (Upper Level Discriminator) Ten-turn potentiometer sets maximum input amplitude acceptance level, continuously adjustable from 8.2V to 20 mV.
- RTP Seven position rotary switch selects RTP or DT after peak with values of 0.5, 1.5, 3, 6, 8, 16 or 25 mS. This

allows considerable delayed coincidence to be achieved even if short pulses are being analysed.
- BASELINE (Zero Energy Intercept) Twenty-turn control changes the "zero level" from 0 to 200 mV

- SINGLE CHANNEL ANALYSER The pulses falling within the window of variable width selectable by appropriate adjustment of the lower and upper level discriminators generate a pulse available at the rear panel BNC connector, having the following characteristics:

  False: OV
  True: 5V

- SVA MODE (Sample Voltage Analysis): In the sample Voltage Analysis mode the ADC samples and converts slowly varying DC input signals to the equivalent digital value. The sample time is 0.5 mS. On expiration of this time the ADC converts the sample to its digital equivalent. Sampling pulse requirements:
- False 0V<VF<0,5
- True 3V<VT<5
- Width ³100nS

INTERFACE SPECIFICATIONS

- 13 Data Lines with 3 state output gates to computer
- OUTPUT DATA ENABLE (DATA REQUEST) line from computer
- DATA READY line to a computer
- DATA ACCEPTED line from computer
- RUN/STOP line
- Power requirements +24V - 0.11 A; -24V - 0.11A; +6V - 0.9A; -6V - 0.14A; +12V - 0.006A; DC voltages as per "Standard Nuclear Instruments Modules TID 20893" (Rev. 2 Jan. 1968)
- Operating temperature 5 to 45 °C range (Because of the high density circuit package, ample air flow must be assured to provide adequate cooling as specified in "Standard Nuclear Instruments Modules" Rev. 2 Jan. 1968 pag. 7 Point 5)
- Dimensions: Single two-width NIM standard module
- Weight: 2 Kg.

OPTIONS AVAILABLE

- Double-ended 100 Ohms Line Drivers and Receivers on the J3 connector lines available on request.
- Cable for connection to Canberra MCB available on request